METHOD AND APPARATUS FOR COHERENT MEMORY STRUCTURE OF HETEROGENEOUS PROCESSOR SYSTEMS

ABSTRACT OF DISCLOSURE

Disclosed is a coherent cache system that operates in conjunction with non-homogeneous processing units. A set of processing units of a first configuration has conventional cache and directly accesses common or shared system physical and virtual address memory through the use of a conventional MMU (Memory Management Unit). Additional processors of a different configuration and/or other devices that need to access system memory are configured to store accessed data in compatible caches. Each of the caches is compatible with a given protocol coherent memory management bus interspersed between the caches and the system memory.